Amendments to the Claims

1. (*Currently Amended*) A method of reducing inter-symbol interference occurring at the digital to analog conversion of a one-bit digital signal stream, the generation of said one-bit digital signal stream ~~(So) comprising the steps of~~ comprising the steps of:

converting an input signal to said one-bit digital signal stream with a sigma-delta configuration ~~(SD)~~ of a low pass filter ~~(F)~~ having an output coupled to the input of a quantizer ~~(Q)~~ whose output is fed back to the input of the low pass filter,

characterized by generating a control signal ~~(Sc)~~ that is representative of the density of the edges of the one-bit digital signal stream at the output ~~(0)~~ of the quantizer,

multiplying the control signal ~~(Sc)~~ with said one-bit digital signal stream ~~(So)~~ and

applying the result of the multiplication together with the output of the low pass filter (F) to the input of the quantizer ~~(Q)~~.

2. (*Currently Amended*) A one-bit sigma-delta converter for converting an input signal ~~(SI)~~ to a one-bit digital signal stream ~~(So)~~, said converter comprising

a quantizer ~~(Q)~~ with an input and an output,

a low pass filter ~~(F)~~ whose output is coupled to the input of the quantizer and whose input is coupled to the output of the quantizer, thereby constituting a feedback-arrangement with the quantizer,

means ~~(PI)~~ to supply the input signal ~~(SI)~~ to the feedback arrangement and

means ~~(0)~~ to derive the one-bit digital signal stream from the output of the quantizer, characterized by an edge-density controller ~~(G)~~ connected to the output ~~(0)~~ of the quantizer for providing a control signal ~~(Sc)~~ indicative of the density of the edges of the one-bit digital signal stream ~~(So)~~,

a multiplier ~~(M)~~ for multiplying said control signal ~~(Sc)~~ with the one-bit digital signal stream ~~(So)~~ of the quantizer and

means ~~(P2)~~ for applying the output of the multiplier to the input of the quantizer.

3. (*Currently Amended*) A one-bit sigma-delta converter as claimed in claim 2 characterized in that the edge-density controller ~~(G)~~ comprises

_____an edge-extractor ~~(E)~~ connected to receive the one-bit digital signal stream ~~(So)~~ of the quantizer, and

_____a second low pass filter ~~(N)~~ receiving the output signal ~~(SE)~~ of the edge-extractor and providing said control signal ~~(Sc)~~.

4. (*Currently Amended*) A one-bit sigma-delta converter as claimed in claim 3 characterized by a reference signal source ~~(Vp)~~ connected to the second low pass filter ~~(N)~~ for referencing the level of the control signal ~~(Sc)~~.

5. (*Currently Amended*) A one-bit sigma-delta converter as claimed in claim 3 characterized in that the second low pass filter ~~(N)~~ is an integrator and that the reference signal is applied with a polarity opposite to that of the edge-extractor pulses to the input of the integrator.

6. (*Currently Amended*) A multi-bit sigma-delta converter for converting an input signal ~~(SI)~~ to a multi-bit digital signal, <u>said converter comprising</u> <u>said converter comprising:</u>

_____a plurality of interconnected one-bit sigma-delta converters each with a low pass filter ~~(F)~~ in feedback arrangement with one of a plurality ~~(VQ)~~ of interconnected quantizer means,

_____means to supply the input signal to said plurality of quantizer means and means to derive the multi-bit digital signal from the outputs ~~(01, 02,03)~~ of the plurality of quantizer means, characterized in that each of the outputs of the plurality of quantizer means is connected to an edge-density controller ~~(G)~~ for providing a control signal indicative of the edges of the one-bit digital stream at said output,

_____a multiplier ~~(M)~~ for multiplying said control signal with the one-bit digital stream of said output and

_____means ~~(P2)~~ for applying the result of the multiplication to the respective input of the quantizer means ~~(VQ)~~.

7. (*Currently Amended*) A storage medium ~~(J)~~ having stored thereon at least one signal track in one-bit digital stream format, characterized in that the number of clock periods comprising an edge in the one-bit digital stream of said signal track is less than 40% of the total number of clock periods of the one-bit digital stream of said signal track.